Remarks:

In the Office Action mailed on November 26, 2007, the Examiner rejected claims 1-33 and objected to Claims 10, 32 and 33.

Applicants amend claims 1, 3, 4, 6, 8, 10-13, 16-18, 25, 27, 29 and 32-33 herein.

New claims 34-39 have been added. These claims new dependent claims in the hierarchies rooted at claims 11, 12, and 13, respectively. These new claims have parallels in Claims 32 and 33 and are supported, for example, by Paragraphs 0024 and 0035 of the Specification. Accordingly, no new matter has been added.

Claims 1-39 are pending in the application.

Interview

On February 26, 2008, the undersigned representative of Applicants and the Examiner discussed the application in a telephonic interview. Applicants thank the Examiner for that opportunity to discuss the case.

Prior to the interview, Applicants provided the Examiner with a copy of the claim amendments made herein. The Examiner indicated that the 35 USC 112 rejections would be withdrawn in light of these amendments.

The undersigned explained the claims using Figures 2 and 5 of the patent application to illustrate the mapping of a logical area to a plurality of physical areas and the progression of active physical area in response to the three different categories of write operations illustrated in Figure 5 and discussed in the accompanying description in the Specification. Furthermore, the undersigned explained his understanding of the Ban reference and how Ban could not teach or suggest such a structure and method of operation as Ban appears to have a one-to-one mapping of logical units to physical units and that that mapping can change.

The Examiner made note of these arguments but, reciting lack of authority and shortness of time to prepare, did not commit to a position with respect to the presented arguments.

The Examiner and the undersigned also discussed a lack of clarity in the drawings. While this issue had not been raised by the Examiner, in discussing Figure 5 it became evident that some of the bolding of characters are not as clear as could be desired. The undersigned agreed to provide clearer drawings, but will defer doing so for the time being. The undersigned expects to be able to provide revised drawings well-before the next action by the Examiner.

The Claims

Claim Objections

Claims 10, 32, and 33 were objected for informalities that the examiner correctly assumed to be typographical errors. Applicants have amended these claims to correct the errors. Accordingly, withdrawal of the informalities objection.

35 USC 112, first and second paragraph

Claims 1-33 were rejected under 35 USC 112, first and second paragraph as failing to copy with the written description requirement and for being indefinite for failing to comply with the written description requirement. Applicants amend the claims herein. As indicated above, the Examiner has had an opportunity to review these claim amendments and has indicated that these rejections will be withdrawn.

35 USC 103

Claims 3, 7-8, 18, 24 and 28-29 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban (WO/94/20906) hereinafter Ban as applied to claims 1-2, 13 and 23 above and in further view of Assar et al (WO

95/10083 hereinafter Assar). Claims 4 and 25 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban as applied to claims 1 and 13 and further in view of Mennecart (WO 01/88926 A1) hereinafter Mennecart. Claims 5 and 26 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban as applied to claims 2 and 13 and further in view of Hazen et al (WO 99/35650) hereinafter Hazen. Claims 6 and 27 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Hazen as applied to claims 5 and 26 and in view of Lipovski (US 5,758,148) hereinafter Lipovski. Claims 9-10 and 30-31 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban as applied to claims 1-2 and 13 and further in view of Kuo (US 4,763,305) hereinafter Kuo. Claim 12 is rejected under 35 U.S.C.103 (a) as unpatentable over Ban and further in view of Robinson et al (US 5,375,222). Claims 14-17 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Hazen as applied to claims 5 and 6 and further in view of Assar. Claims 19-20 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Hazen as applied to claim 5 and 6 and further in view of Kuo. Claims 21-22 is rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Assar as applied to claim 7 and further in view of Kuo.

Ban

While Ban, like applicant, addresses writing into a flash memory, Ban's approach is quite different from the method described and claimed by applicants.

In a flash type memory data is written by merely turning bits having the value zero to the value one. That, of course, only works if the bits that are to be zero after the write were already zero before the write. Otherwise, the data location has to first be erased. Thus, writes normally involves zeroing out the data location and then writing the required one bits. Applicants address the issue that erasing a flash memory is a very

costly operation in contrast to write operations. Thus, when an operation is performed that requires an erase operation, that operation is costly.

Applicant's solution is to associate a plurality of physical areas of the memory to each logical area. Then writes can be made by successively writing to these areas of memory that are each associated with the same logical area. Erase operations can be made when convenient, e.g., during idle moments. Thus, the write operations are generally optimized.

Applicants thus claim, "defining a mirror area divided in at least two physical areas of said memory designed to contain a same logical area for storing a content" (Claim 1). One of the areas is "designat[ed] ... as being an active physical area", and "during a write to said logical area, programming the content of said logical are into the active physical area." (Claim 1).

Ban's solution does not teach or suggest these steps. While Ban organizes the memory into blocks and units, in writing to a unit, if a logical address is not free, an available free address is located. Ban, Page 9, lines 14-15. To reclaim memory, periodically all active blocks of one unit is copied into a unit, the TRANSFER unit, and the originating unit is flash erased. Ban, page 9, lines 23-26. However, there is no association of multiple physical areas of memory to a particular logical area as is claimed herein. Ban does not disclose or suggest a stationary association of a group of physical areas to a same and unique logical area.

Ban never discloses or suggests "associating at least two physical areas of the said memory ... with a same and unique logical area for storing a content." In Fig. 4, element 35, "a logical unit table 35 translates *the* logical unit number to *a* physical unit number for *the* logical unit" (Ban, page 8, lines 8-9) and "the logical address is mapped to *a* physical address in the flash memory" (page 8, lines 22-23). Thus, it is clear that there is a one-to-one mapping in Ban between logical units and physical units. Nowhere does Ban say anything to the contrary.

In the response to arguments section, the Examiner indicated disagreement with Applicant in regards to Ban teaching a one-to-one mapping. The Examiner pointed to Ban's statement that "Here it should be noted, the virtual address space is not necessarily the same size as the physical address space. (Page 2, lines 26-28)." (Office Action, Page 24). Applicants disagree that that statement contradicts Applicants' position vis-à-vis Ban.

Typically virtual addressing is used precisely to deal with limits in a physical address space. Many addressing schemes allow for addressing much larger spaces than the available physical space. Mapping virtual addresses to physical addresses in a clever way addresses that mismatch between the addressing capabilities of a machine versus the actual available physical space.

That makes sense in the context of Ban as well. Ban goes on to say that "[associated] in the table with each virtual block address there is a corresponding physical address." (Ban, Page 3, Lines 9-11). Thus, for each virtual block there is one physical block. In a virtual addressing scheme, the virtual space can be larger than the physical area available. Therefore, for each virtual address used there needs to be a mapping to a physical area. Implicit is that there cannot be more virtual space in active use than there is physical space available because if there were, more space would be in use than is available.

While there can be a difference in the virtual space and the physical space, there is no indication that multiple physical address blocks are used for the same virtual address block. That is not surprising because Ban's system operates on a different principle.

Ban describes that when writing to a physical block that cannot be written to, "an unwritten block is therefore located and written to. The virtual memory map is changed so that the unwritten physical block is mapped to the original virtual address and original physical block is

denoted as unusable." (Ban, Page 3, Lines 19-24). Thus, Ban's method for dealing with writing to physical blocks that have already been written is to find a new block and to manage this block-allocation through a memory map.

However, that does not address the notion of Applicants' claims that "a mirror area [is] divided in at least two physical areas ... and designed to contain a same logical area." Implicit in this claim is a fixed association between the at least two physical areas and the logical area. That is in clear contradistinction to Ban where there is an explicit one-to-one mapping between virtual areas, logical areas, and physical areas (see Figure 4) and a dynamic allocation of new areas when there is a need to write to an already written-to physical block.

The Examiner further argues that "it can be reasonably interpreted that the physical units can be the physical byte addresses from the physical block, and the logical/virtual block corresponds to 512 byte physical block (address which denotes a 512 byte range, ie, beginning address + offset = physical block address) or 512 single physical byte addresses (page 3, line 1-29). And the zones and logical units (FIG. 2, 3, 4, & 7) can be reasonably interpreted to be logical areas, which are made up of a plurality of blocks and physical areas." (Office Action, Page 24, Lines 12-18). Applicants disagree with this reading of Ban.

While one could read logical area and physical area broadly to cover different divisions of memory, in Applicants' claims, there is still a stated mapping between one logical area and at least two physical areas. That means that there would be a bit-for-bit mapping between the two. This can be seen advantageously in Figure 5 wherein the logical area to be written to (dashed area) corresponds bit-for-bit to the physical areas ZPn and ZPn+1. The fact that Ban's memory is composed of zones and logical units that are made up of a plurality of blocks and physical areas does not provide that bit-for-bit mirroring. If it did, a virtual address/logical

address would correspond to multiple addresses in the physical areas. However, as is evident from Figure 4, each virtual address/logical address correspond to exactly one physical address.

An advantage of Applicants' claimed invention in comparison to Ban is that in Applicants' solution there is not a need for Ban's mechanism for releasing physical areas for use by other logical areas. Further, because each logical area would have at least two physical areas associated therewith, Applicants' memory would be faster than a memory with dynamic allocation of physical areas such as proposed by Ban.

Based on the foregoing arguments, Applicants respectfully submit that Claim 1 is not obvious over Ban and should be allowed.

Claims 11, 12, and 13 recite analogous limitations and should be allowed for, at least, the same reasons given in support of Claim 1.

Assar, Mennecart, Hazen, Lipovski, and Kuo are cited by the Examiner for propositions other than those argued hereinabove. None of these references teach or suggest "associating at least two physical areas of said memory, called mirror areas, with a same and unique logical area for storing a content; designating one of the physical areas as being an active physical area; and during a write to said logical area, programming the content of said logical area into the active physical area" (Claim 1 and analogous in the other independent claims). Therefore, Claim 1 and the other independent claims are patentable over these references taken singly, or in any combination including or not including Ban.

Therefore, because all the dependent claims depend from the independent claims, incorporate all the limitations thereof and provide further unique and non-obvious combinations, the dependent claims are patentable for, at least, the reasons given in support of the independent claims. (Applicants reserve the right to argue the independent

patentability of the various dependent claims in response to any further rejection of these claims).

The application is now deemed to be in condition for allowance and notice to that effect is solicited.

CONCLUSION

It is submitted that all of the claims now in the application are allowable. Applicants respectfully request consideration of the application and claims and its early allowance. If the Examiner believes that the prosecution of the application would be facilitated by a telephonic interview, Applicants invite the Examiner to contact the undersigned at the number given below.

Applicants respectfully request that a timely Notice of Allowance be issued in this application.

Respectfully submitted,

Date: February 26, 2008

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